BACKGROUNDERS
Press Information Bureau
Government of India

Design Linked Incentive Scheme

Catalyzing India's Semiconductor Design Ecosystem

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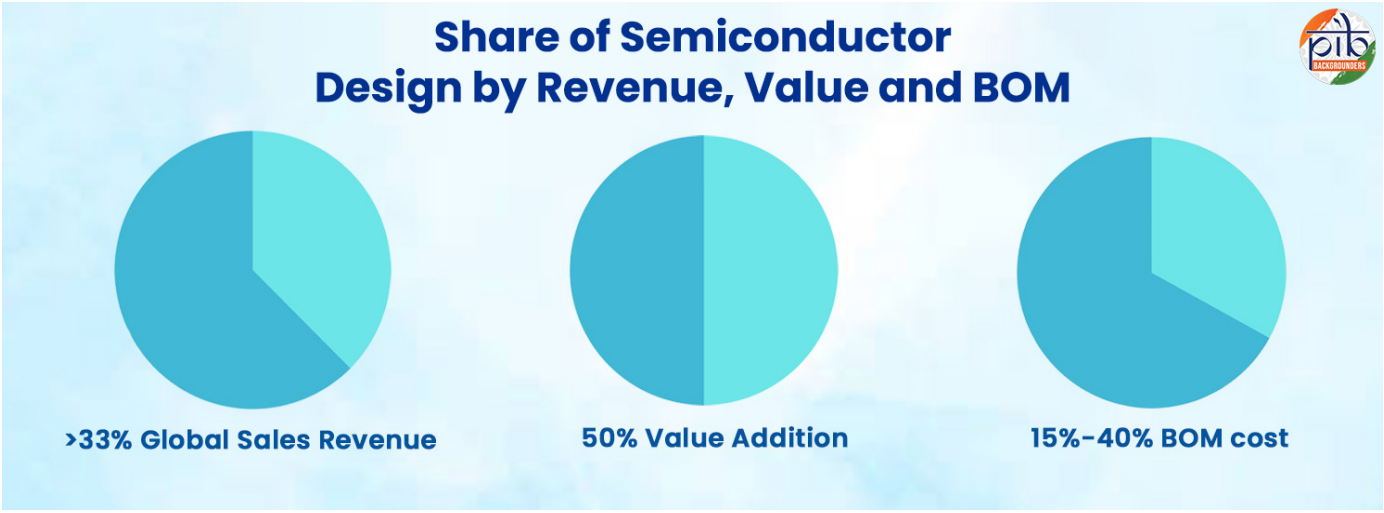
Key Takeaways

- Semiconductor chip **design is the main value driver**, contributing up to **50% of value addition**, **20–50% of Bill of Materials cost (BOM)**, and **30–35% of global semiconductor sales** via the fabless segment.
- **MeitY's Design Linked Incentive (DLI) Scheme** under the **Semicon India Programme** aims to build a **self-reliant, globally competitive chip design ecosystem**.
- **24 DLI-supported chip design projects** target **strategic sectors** including video surveillance, drone detection, energy metering, microprocessors, satellite communications, and IoT SoCs.
- **DLI supported projects are scaling rapidly**, with **16 tape-outs**, **6 ASICs chips**, **10 patents**, **1,000+ engineers engaged**, and **over 3× private investment leveraged**.

Introduction

India is rapidly advancing its semiconductor ambitions, recognizing semiconductor chips as critical enablers of healthcare, transport, communications, defence, space, and emerging digital infrastructure. With accelerating digitalization and automation, global demand for semiconductor chips is rising sharply. In response, the Government of India, through the **Semicon India Programme** and the **India Semiconductor Mission (ISM),** is strengthening the domestic semiconductor ecosystem and supply chain. However, semiconductor manufacturing remains concentrated in a limited number of geographies, making global supply chains highly fragile and vulnerable to disruptions. This underscores the urgent need to diversify the global manufacturing base, with India increasingly emerging as a strategic and reliable player in the global semiconductor landscape.



Did You Know: Fabless chip design is the key enabler of semiconductor value chain

In the electronics value chain, fabless semiconductor companies hold the highest strategic value because they design the chips that drive product intelligence, efficiency, and security. While fabs manufacture silicon and EMS firms assemble devices, more than half of a semiconductor's value comes from design and IP, not physical production. Fabless semiconductor design models generate high value addition with relatively modest capital expenditure, as design and IP contribute disproportionately to product economic value.

Without strong fabless capability, a nation remains dependent on imported core technologies even if electronics are manufactured locally. Building a robust fabless ecosystem therefore enables India to own the most critical layer of the value chain, retain intellectual property, reduce imports, attract manufacturing, and establish long-term technological leadership.

DLI Scheme

The Design Linked Incentive (DLI) Scheme is a key instrument in advancing India's ambition to develop a strong fabless capability. The scheme is implemented by the Ministry of Electronics and Information Technology (MeitY) under the Semicon India Programme to catalyze a strong, self-reliant chip design ecosystem by providing financial incentives and access to advanced design infrastructure for domestic startups and MSMEs.

The DLI Scheme supports semiconductor design across the full lifecycle—from design and development to deployment—covering Integrated Circuits (ICs), chipsets, Systems-on-Chip (SoCs), systems and IP cores. By promoting indigenous semiconductor content and intellectual property in electronic products, the scheme aims to reduce import dependence, strengthen supply chain resilience, and enhance domestic value addition.

ELIGIBILITY UNDER THE DLI SCHEME
Start-ups and MSMEs are eligible for financial incentives and design infrastructure support for semiconductor product design & deployment and **other domestic companies** are eligible for financial incentives for deploying semiconductor designs. • **MSMEs:** Defined according to the **Ministry of Micro, Small and Medium Enterprises notification**, 1 June 2020. • **Startups:** Defined as per the Department for Promotion of Industry and Internal Trade (**DPIIT) notification**, 19 February 2019. • **Domestic companies:** Defined as those which are owned by **resident Indian citizens**, as per the Foreign Direct Investment (FDI) Policy Circular, 2017 or extant norms.

Financial Incentives and Design Infrastructure Support under DLI

FINANCIAL INCENTIVES	
Product Design Linked Incentive	**Deployment Linked Incentive**
➢ Reimbursement of up to 50% of eligible expenditure.	➢ Incentives of 6% to 4% of net sales turnover are provided for five years.

➢ The reimbursement is capped at ₹15 crore per application. ➢ The support is available to entities involved in semiconductor design for: Integrated Circuits (ICs) Chipsets Systems on Chips (SoCs) Systems & IP Cores Semiconductor-linked designs.	➢ The incentive is capped at ₹30 crore per application. ➢ The minimum cumulative net sales required over Years 1–5 is 1 crore for startups/ ₹ MSMEs and 5 crore for other domestic companies. ➢ The design must be successfully deployed in electronic products.

DESIGN INFRASTRUCTURE SUPPORT

C-DAC has established the ChipIN Centre under the DLI Scheme to facilitate the design infrastructure support to approved companies::

- **National EDA (Electronic Design Automation) Tool Grid:** Remote access to the centralized facility of advance EDA tools for chip design activities will be provided to start-ups and MSMEs.
- **IP Core repository:** Flexible access to the repository of IP Cores for SoC design activities.
- **MPW Prototyping support:** Fiscal support for fabricating the design in MPW manner at semiconductor foundries.
- **Post-silicon validation support:** Fiscal support for testing and validation of the fabricated ASIC and silicon bring-up activities.

Programme Highlights & Key Achievements of DLI

Since its launch in December 2021, the Design Linked Incentive (DLI) Scheme has been instrumental in shaping a stronger and more self-reliant semiconductor design ecosystem in India. By extending financial incentives, access to advanced design tools, and prototyping support to companies, startups, and academic institutions, the scheme enables innovators to progress seamlessly from ideas to actual silicon chips. This ecosystem-driven approach has been anchored by the creation of shared national infrastructure for chip design.

A key pillar of this infrastructure is the ChipIN Centre, which has democratized access to advanced EDA tools for chip design for about 1 lakh engineers and students across 400 organizations nationwide—making it the world's largest user base of a centralized chip design facility. This includes support to around 305 academic institutions under the Chips to Start-up (C2S) Programme and 95 startups under the DLI Scheme, significantly reducing entry barriers for early-stage innovators.

Complementing this effort, India's shared EDA Grid—a national platform offering high-end chip design software—**has recorded 54,03,005 hours of cumulative usage by 95 supported start-ups as of 2nd January 2026**, reflecting strong adoption by startups, MSMEs, and researchers across all States.

These enabling measures have translated into tangible outcomes for the domestic startup ecosystem. Supported companies under the DLI Scheme have moved from innovation to execution, with ten patents filed, **16 chip-design tape-outs completed**, and **six semiconductor chips successfully fabricated**—marking critical milestones from concept to silicon. In parallel, **over 1,000 specialised engineers have been trained or engaged through DLI-supported projects**, strengthening India's design talent base. Beneficiaries have also developed more than **140 reusable semiconductor IP cores**, which serve as critical enablers for advanced chip development.

Building on these successes, the DLI Scheme is now driving the transition from design validation to productization, enabling start-ups and MSMEs to move toward volume manufacturing, system integration, and market deployment. This evolving ecosystem not only strengthens India's domestic semiconductor capabilities but also positions the country as a credible player in global chip design and innovation.

Key Institutional Frameworks for Semiconductor Design

India's semiconductor ecosystem is being strengthened through a coordinated institutional framework that combines policy leadership, investment support, capacity building, and indigenous technology development. Key programmes and agencies provide end-to-end backing—from incentivizing chip design and manufacturing to developing skilled talent and fostering open-source microprocessor architectures—ensuring India's progression toward a self-reliant and globally competitive semiconductor design ecosystem.

1. **Ministry of Electronics and Information Technology (MeitY):** MeitY leads national semiconductor initiatives, provides policy direction, and anchors schemes. It also coordinates institutional and industry partnerships to strengthen India's chip design and manufacturing ecosystem. MeitY has announced the Design Linked Incentive (DLI) Scheme; aims to offset the existing disabilities in India's domestic semiconductor design industry. It seeks to help Indian companies move up the semiconductor value chain.

2. **Semicon India Programme (SIM):** With an outlay of ₹76,000 crore, the programme supports investments in semiconductor and display manufacturing as well as the design ecosystem. The DLI Scheme operates under this programme, ensuring end-to-end backing for design, fabrication and productisation. C-DAC, a premier R&D organization of the MeitY, is responsible for implementation of the DLI Scheme as Nodal Agency.

3. **Chips to Startup (C2S) Programme**: C2S is an umbrella capacity building programme initiated at academic organizations spread across the country to generate 85 thousand number of industry-ready manpower at B.Tech, M.Tech, and PhD levels specialized in semiconductor chip design.

4. **Microprocessor Development Programme**: The Microprocessor Development Programme, initiated at C-DAC, IIT Madras and IIT Bombay has resulted into design, development and fabrication of open-source architecture-based family of microprocessors viz. VEGA12, SHAKTI13 and AJIT microprocessors as a step towards self-reliance.

Together, these institutional initiatives create a robust foundation for India's semiconductor ambitions, enabling startups, MSMEs, and academic institutions to innovate and scale. By bridging the gap from research to productization, they are driving self-reliance, enhancing global competitiveness, and positioning India as a strategic player in the global semiconductor landscape.

Success Stories of India's Design Linked Incentive (DLI) Scheme

Under the DLI scheme, **24 chip-design projects have been sanctioned across areas such as video surveillance, drone detection, energy meters, microprocessors, satellite communications, and broadband and IoT SoCs.** Additionally, **95 companies have received access to industry-grade EDA tools**, significantly reducing design and infrastructure costs for Indian chip design startups. Among the beneficiaries, following companies stands out as leading examples of how the DLI Scheme is nurturing world-class semiconductor innovation:

- **Vervesemi Microelectronics**, with a **strong portfolio of 110+ semiconductor IPs, 25 integrated circuit (IC) product variants, 10 granted patents, and 5 trade secrets** is developing motor-control chips for a wide range of applications, including consumer appliances such as fans, coolers, mixer grinders, air conditioners, washing machines, and drones, as well as automotive applications like e-scooters and e-rickshaws. These chips support a unique class of BLDC motors. Vervesemi has **completed pilot-lot sampling for two chips, with a third chip expected from the foundry later this year** and has several global customers already engaged in product development using the existing chips.

- **InCore Semiconductors** is focused on the design and development of indigenous RISC-V microprocessor IPs and SoC design automation tools, with the ultimate goal of building India's most powerful embedded processor, Dolomite, targeted at entry-level smartphones and edge-AI applications. InCore's portfolio of processor IP cores is silicon-proven across multiple customer chips, fabricated at technology nodes ranging from 180 nm to 16 nm, and aims to reduce India's dependence on imported CPU IP while enabling strategic and commercial applications.

- **Netrasemi is** focused on **designing AI-capable SoCs for CCTV secure surveillance, smart sensors, robotics and drones, and mobility applications**. The company has successfully taped out India's first indigenously designed AI SoC in an advanced 12 nm process node, integrating in-house AI/ML accelerators, vision processing, and video engines. **Netrasemi is also backed by the largest private venture capital funding to date for an Indian semiconductor company and has a series of design tape-outs** lined up next year, ranging from low-end to high-complexity surveillance SoCs.

- **Aheesa Digital Innovations** is developing Vihaan, an indigenous fiber-broadband solution used to connect homes and businesses to high-speed fiber networks. **Vihaan is built around an indigenous VEGA processor–based Gigabit Passive Optical Network (GPON) Optical Network Terminal (ONT) and Network SoC**, which integrates fiber termination, data processing, and network management functions into a single chip. This enables reliable, secure, and cost-effective broadband connectivity. They are on track to introduce reference platforms for customer exploration in 2026.

- **AAGYAVISION is designing advanced radar-on-chip** that operate reliably in all weather conditions, driving advancements in safety, security, smart infrastructure, edge computing, and emerging 6G sensor networks as well as critical application like drone detection.

The success stories illustrate how the DLI Scheme is converting indigenous chip design capabilities into silicon-proven, market-ready products. By supporting advanced design, prototyping, and commercialization, the scheme is strengthening India's technological self-reliance and its position in the global semiconductor design ecosystem.

Conclusion

The Design Linked Incentive (DLI) Scheme is critical to anchoring India in the most strategic and value-intensive segment of the global semiconductor value chain—chip design. By reducing dependence on imported semiconductor IPs and chips, strengthening resilience against geopolitical and supply-chain disruptions, and ensuring assured access to critical technologies for defence, telecom, AI and mobility, DLI lays the foundation for strategic autonomy and long-term economic growth. The scheme also enables high-value growth by translating deep-tech innovation into globally competitive products, fostering startups and MSMEs, and building a highly skilled engineering workforce.

These outcomes are already evident, with DLI-supported firms achieving multiple chip tape-outs, silicon-proven designs, patents, reusable IPs, trained talent and operational design infrastructure, demonstrating tangible on-ground impact. As the ecosystem enters the productization phase, silicon-validated designs are moving toward volume manufacturing, system integration and market deployment, positioning Indian companies as credible global suppliers while strengthening domestic supply chains and reinforcing India's self-reliant semiconductor ecosystem.

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